AMENDMENT

In the Specification:

Please replace paragraph 2 on page 5 with the following:

The illustrative embodiment of the present invention provides a sensor that indicates whether it is functioning properly, whether it is sensing or not and a response to a physical stimulus. In the illustrative embodiment a sensor is adapted to have a serial interface to report three data values in response to a control signal that initiates a sensing process. A first data value indicates whether a sensing operation is in process, a second data value represents a response to the sensed physical stimulus and a third data value indicates whether the sensor is functioning properly.

Please replace paragraph 4 on page 5 which continues onto page 6 with the following:

Figure 1 is a block diagram of an exemplary integrated circuit 12 that is suitable for practicing the illustrative embodiment of the present invention. The sensor 14 is an active device within the exemplary integrated circuit 12. The sensor 14 includes a register to hold a response to a physical stimulus. Coupled to the sensor 14 are the clock input node 24, the power input node 22, the ground node 20, the input node 18 and the output node 16. Input node 18 and output node 16 provide the sensor 14 with an interface external to the exemplary integrated circuit 12. The power input node 22 is tied to a voltage source that can be controlled independently of the voltage source supplying a voltage level to the remainder of the active devices within the exemplary integrated circuit 12. The clock node 24 receives a clock signal 37 and is ~~also~~ coupled to a clock source or driver that can be controlled independently of any other clock source driver

within the exemplary integrated circuit 12. As a consequence, the sensor 14 can be operated independently of the exemplary integrated circuit 12 and therefore used to determine a base line temperature of the exemplary integrated circuit 12 for calibration purposes. In this manner, the sensor 14 can be calibrated without having to compensate for the thermal affects of having one or more other active elements within the exemplary integrated circuit 12 active during baselining.

Please replace second full paragraph on page 7 which continues to the top of page 8 with the following:

Figure 2 is a waveform diagram that illustrates the digital signals communicated to the input node 18, to the clock node 37, and from the output node 16. The input signal 30 acts as a reset signal to reset the sensor 14 and initiate a sensing operation by the sensor 14. The output signal 32 is a digital signal that toggles between a logic "0" level and a logic "1" level to communicate a ~~the~~ first data value 31, a ~~the~~ second data value 33 and a ~~the~~ third data value 35 of the sensor 14 in serial fashion. Clock signal 37 asserted on clock node 24 is provided for illustrative purposes to help facilitate explanation of the invention and is not meant to limit the scope of the present invention. For example, those skilled in the art will readily recognize that the input signal 30 and the output signal 32 can transition states based on a rising edge of the clock signal 37 or a falling edge of the clock signal 37. Furthermore, those skilled in the art will readily recognize that the illustrated values the first data value 31, the second data value 33 and the third data value 35 are not limited by the number of clock cycles illustrated.

Figure 3 illustrates the steps taken by the sensor 14 to report a sensed physical stimulus. Upon power up of the sensor 14, the state of the sensor is unknown. As such,

the input signal 30 is held asserted to a logic level "0" at the input node 18 to force the sensor 14 to its initial or starting state. By forcing the sensor 14 to its starting state the content of the register 15 is reset. The sensor 14 remains in this state until the input signal 30 asserted at the input node 18 rises to a logic "1" level following at least one clock cycle of the clock signal asserted 37 on the clock input node 24. Those skilled in the art will recognize that sensor 14 can be configured so that when the input signal 30 is asserted to a logic "1" level at the input node 18 to force the sensor 14 to its initial or starting state. Moreover, those skilled in the art will recognize that the input signal 30 can be asserted to a logic "0" level at any time after the power on reset to again force the sensor 14 to its initial or starting state.

Please replace the first full paragraph on page 8 with the following:

Once the input signal 30 rises to a logic "1" level on the input node 18, the sensor 14 initiates sensing a physical stimulus within the exemplary integrated circuit 12 to obtain an absolute or relative quantitative measurement (step 52 in Figure 3). During the sensing process of the sensor 14, the input signal 30 at the input node 18 is held at a logic "1" level and the output signal 32 assertsed the first data value 31 on the output node 16 ~~is also held at a logic "1" level~~ (step 52 in Figure 3). The logic "1" level of the first data valve 31 of the output signal 32 asserted on the output node 16 indicates that the sensor 14 is obtaining a measurement of a physical stimulus, such as the internal temperature of the exemplary integrated circuit 12. Those skilled in the art will recognize that the sensor 14 can be configured so as the output signal 32 asserts a logic "0" level on the output node 16 to provide the first data value that indicates that the sensor 14 is obtaining a measurement of a physical stimulus, such as the internal temperature of the exemplary

integrated circuit 12. After a fixed number of clock cycles on the clock input node 24, the sensor 14 places a measurement value of the physical stimulus into the register 15 and deasserts the output signal 32 on the output node 16 for at least one clock cycle of the clock signal 37 asserted on the clock input node 24 (step 54 in Figure 3).

Please replace the second full paragraph on page 8 which continues on page 9 with the following:

After one clock cycle of the clock signal 37 on the clock input node 24, the sensor 14 shifts the second data value 33 representing the measured value of the physical stimulus out of the register 15 on the output node 16 at a rate of one bit per clock cycle on the clock input node 24 (step 56 in Figure 3). When the sensor has emptied the register 15, the sensor 14 affixes ~~a~~ the third ~~data~~ value 35 to the response and asserts the third data value 35 on the output node 16 at the rate of one bit per clock cycle on the clock input node 24 (step 58 in Figure 3). The third data value 35 provides an indication that the sensor 14 is functioning correctly. As the output signal 32 illustrates, the affixed third data value 35 corresponds to a 010 bit pattern. Nevertheless, those skilled in the art will recognize that the sensor 14 can affix an alternative bit pattern, such as 101 and the third ~~affixed~~ data value 35 asserted by the sensor 14 can precede or follow the assertion of the second ~~measured~~ data value 33 representative of the measured value shifted out of the register 15. Moreover, those skilled in the art will recognize that the bit length of the second data valve 33 (i.e. measured response) can vary depending on the application, the accuracy required and the like.